

What is claimed is:

- 1 1. A voltage controlled oscillator comprising:
2 a tank circuit;
3 a first pair of cross-coupled transistors to receive a first current from the tank
4 circuit; and
5 a second pair of cross-coupled transistors to receive a second current from
6 the tank circuit, wherein the first and second currents are unequal.
- 1 2. The voltage controlled oscillator of claim 1 wherein the first pair of cross-
2 coupled transistors comprises bipolar junction transistors, and the second pair of
3 cross-coupled transistors comprises isolated gate transistors.
- 1 3. The voltage controlled oscillator of claim 2 wherein the second current is
2 greater than the first current.
- 1 4. The voltage controlled oscillator of claim 2 wherein the first current is large
2 enough for the cross-coupled pair of bipolar junction transistors to satisfy a startup
3 condition of the voltage controlled oscillator.
- 1 5. The voltage controlled oscillator of claim 1 wherein the first and second
2 pairs of cross-coupled transistors are manufactured in a SiGe process.
- 1 6. The voltage controlled oscillator of claim 1 wherein the first pair of cross-
2 coupled transistors exhibits a phase noise substantially proportional to current, and
3 the second pair of cross-coupled transistors exhibits a phase noise substantially
4 proportional to transconductance.
- 1 7. The voltage controlled oscillator of claim 6 wherein the second current is
2 larger than the first current.

- 1 8. An apparatus comprising:
2 a first gain device having a first transconductance value;
3 a first current source to provide a first current to the first gain device;
4 a second gain device having a second transconductance value lower than the
5 first transconductance value;
6 a second current source to provide a second current to the second gain
7 device, the second current being larger than the first current; and
8 a load circuit coupled to the first and second gain devices.
- 1 9. The apparatus of claim 8 wherein the first gain device comprises a cross-
2 coupled pair of bipolar junction transistors.
- 1 10. The apparatus of claim 9 wherein the second gain device comprises a cross-
2 coupled pair of isolated gate transistors.
- 1 11. The apparatus of claim 10 wherein the load circuit comprises a tank circuit.
- 1 12. The apparatus of claim 8 wherein the first gain device exhibits a phase noise
2 substantially proportional to the first current.
- 1 13. The apparatus of claim 12 wherein the second gain device exhibits a phase
2 noise substantially proportional to the second transconductance.
- 1 14. A frequency synthesizer comprising:
2 a comparison circuit to compare a reference signal and a frequency divided
3 signal;
4 a prescaler to divide a frequency of an output signal and produce the
5 frequency divided signal; and

6 a voltage controlled oscillator to synthesize the output signal in response to
7 the comparison circuit, the voltage controlled oscillator including a cross-coupled
8 pair of bipolar junction transistors and a cross-coupled pair of isolated gate
9 transistors coupled to a tank circuit.

1 15. The frequency synthesizer of claim 14 wherein the voltage controlled
2 oscillator further includes a first current source coupled to the cross-coupled pair of
3 bipolar junction transistors to provide a first current, and a second current source
4 coupled to the cross-coupled pair of isolated gate transistors to provide a second
5 current.

1 16. The frequency synthesizer of claim 15 wherein the second current is larger
2 than the first current.

1 17. The frequency synthesizer of claim 15 wherein the first current is sized to
2 satisfy a startup condition of the voltage controlled oscillator.

1 18. The frequency synthesizer of claim 17 wherein the second current is sized so
2 a sum of the first and second currents satisfy an output voltage condition.

1 19. An electronic system that includes a direct conversion receiver with an
2 oscillator input port, a directional antenna coupled to the direct conversion receiver,
3 and a frequency synthesizer coupled to the oscillator input port, the frequency
4 synthesizer comprising:

5 a comparison circuit to compare a reference signal and a frequency divided
6 signal;

7 a prescaler to divide a frequency of an output signal and produce the
8 frequency divided signal; and

9 a voltage controlled oscillator to synthesize the output signal in response to
10 the comparison circuit, the voltage controlled oscillator including a cross-coupled

11 pair of bipolar junction transistors and a cross-coupled pair of isolated gate
12 transistors coupled to a tank circuit.

1 20. The electronic system of claim 19 wherein the voltage controlled oscillator
2 further includes a first current source coupled to the cross-coupled pair of bipolar
3 junction transistors to provide a first current, and a second current source coupled to
4 the cross-coupled pair of isolated gate transistors to provide a second current.

1 21. The electronic system of claim 20 wherein the second current is larger than
2 the first current.

1 22. The electronic system of claim 20 wherein the first current is sized to satisfy
2 a startup condition of the voltage controlled oscillator.

1 23. The electronic system of claim 22 wherein the second current is sized so a
2 sum of the first and second currents satisfy an output voltage condition.

1 24. A method comprising:
2 providing a first current to a pair of cross-coupled bipolar junction
3 transistors;
4 providing a second current a pair of cross-coupled metal oxide
5 semiconductor field effect transistors;
6 summing the first and second currents to form a third current; and
7 providing the third current to a tank circuit.

1 25. The method of claim 24 wherein providing a first current comprises
2 providing an adequate current to satisfy a startup condition.

1 26. The method of claim 25 wherein the first current is inadequate to satisfy an
2 output amplitude condition.

1 27. The method of claim 26 wherein providing a second current comprises
2 providing an adequate current for the third current to satisfy the output amplitude
3 condition.